SYSTEM

Product Information

SY8-CYCLONE

CompactPCI® Serial • FPGA Based Universal Networking Platform
PCIe® x4 • 10 x 100Mbps Ethernet

Document No. 8880 • 4 June 2018

General

The SY8-CYCLONE is a CompactPCI® Serial peripheral board, equipped with a powerful FPGA, and up to ten RJ45 connectors for 100BASE-TX Ethernet. With its PCI Express® x4 interface, the Cyclone®-V FPGA can be used e.g. as Ethernet NIC, switch, router, or gateway. Industrial Ethernet real time protocols and custom specific applications may be integrated. As a 4HP front panel width solution the SY8-CYCLONE provides five RJ45 connectors. As an option, the board is available with ten Ethernet ports in a 8HP width front panel. A reference design based on Quartus® is available as starting point for customers.

The Intel® (formerly Altera) 5CGXFC7C6F23I7N Cyclone®-V FPGA operates over the industrial temperature range and contains 150K logic elements, and also hard IPs for the PCI Express® controller. In addition to non-volatile I^2C memory, 512MB DDR3L soldered RAM is wired on-board to the Cyclone®-V FPGA.

As an option, the SY8-CYCLONE card can accommodate a mezzanine module with a secondary identical FPGA. This would allow either safety critical applications by redundancy, or additional logic elements for custom specific solutions.

Feature Summary

General

- PICMG® CompactPCI® Serial (CPCI-S.0) peripheral slot board
- Single Size Eurocard 3U 4HP or 8HP 100x160mm^2
- CompactPCI® Serial backplane connector P1 for up to x4 PCI Express® lanes/link

FPGA

- Intel® (Altera) 5CGXFC7C6F23I7N FPGA
- Hard IP PCI Express® interface
- Industrial temperature range -40°C to +85°C
- Logic elements 150K
- Adaptive logic modules (ALM) 56480
- Register 225920
- Variable-precision DSP blocks 156
- 18 x 18 multiplier 312
- Alternate scalable FPGA devices on request (C4, C5, C9)

Networking

- Five RJ45 front panel Ethernet connectors w. integrated magnetics
- Option additional five RJ45 front panel Ethernet connectors w. mezzanine card
- C80-EXP mezzanine card available (8HP common front panel assembly)
- 100BASE-TX & 10BASE-T Ethernet
- PHYs TLK110, suitable for industrial Ethernet (e.g. EtherCAT, SERCOSIII, VARAN, ProfiNET, Ethernet/IP)
- PHYs wired via RMII I/F to FPGA differential I/O
- FPGA IP based Ethernet MACs (RMII)

Feature Summary

Special Features

- Two mezzanine connectors SC1/SC2 for optional mezzanine card C80-EXP (5 x PHY)
- Scalable networking design 5 x RJ45 w. 4HP front panel width, 10 x RJ45 w. 8HP F/P
- Alternate usage of SC1/SC2 for custom specific I/O
- Mezzanine connector SD1 for C81-SI optional secondary FPGA mezzanine card (scalable FPGA design - single or dual FPGA solution)
- Alternate usage of SD1 for custom specific I/O and test/debug
- Custom specific basic FPGA board and/or mezzanine FPGA module design on request
- Custom specific front I/O mezzanine card design on request (e.g. M12-D connectors)

Applications

- General industrial networking, FPGA programmable
- Ethernet switch and/or Ethernet NIC functionality
- Mixed protocols industrial Ethernet
- Hardware suitable for e.g. EtherCAT, SERCOSIII, VARAN, ProfiNET, Ethernet/IP
- Multiprotocol router, gateway, bridge, firewall, security
- Real time applications
- Edge computing, IIoT
- Data acquisition, data concentrator, data accelerator

Programming Support

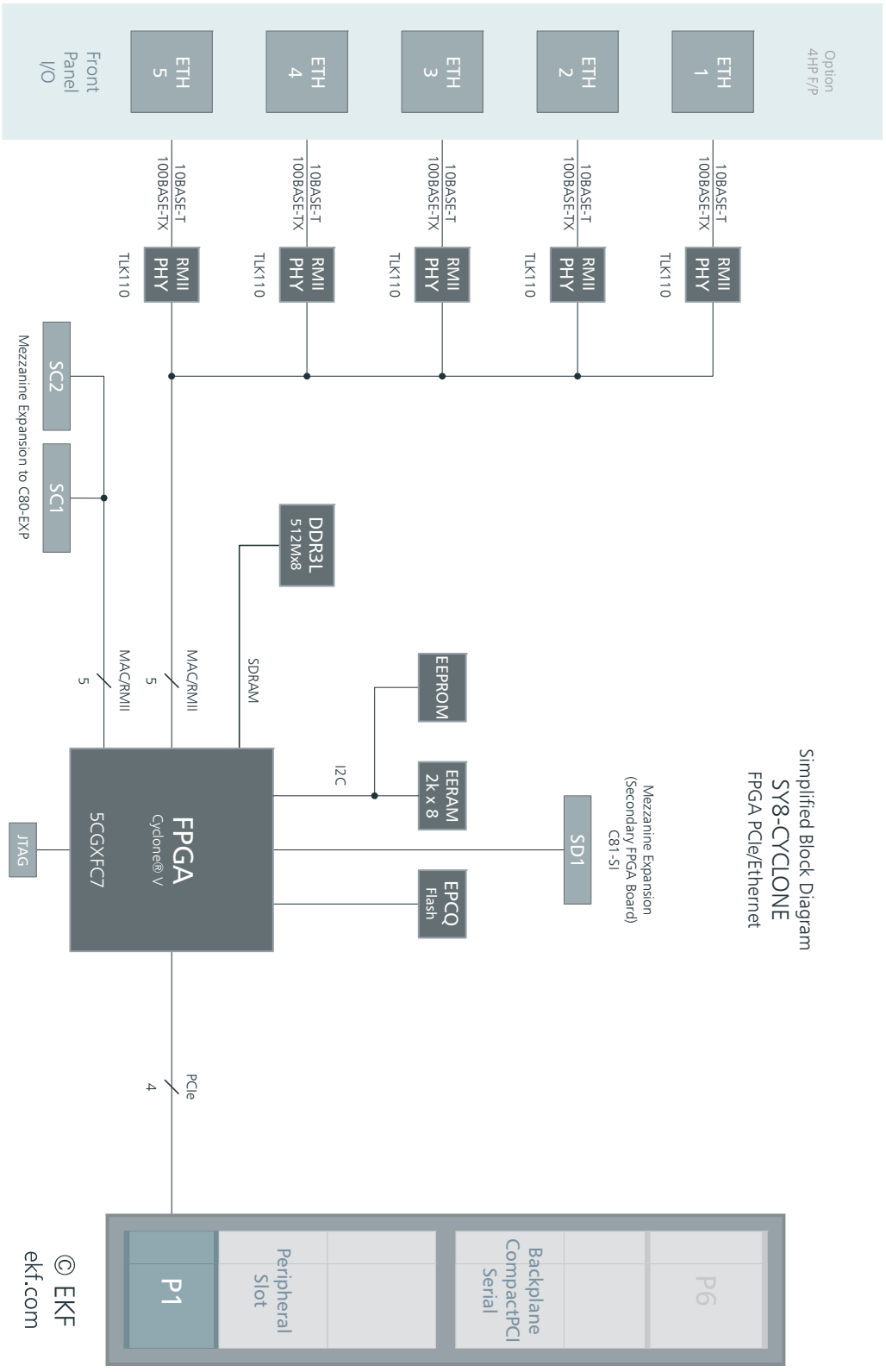
- Reference design available (for Intel® Quartus® Prime design software)
- Linux test tool available
- Custom specific FPGA programming on request

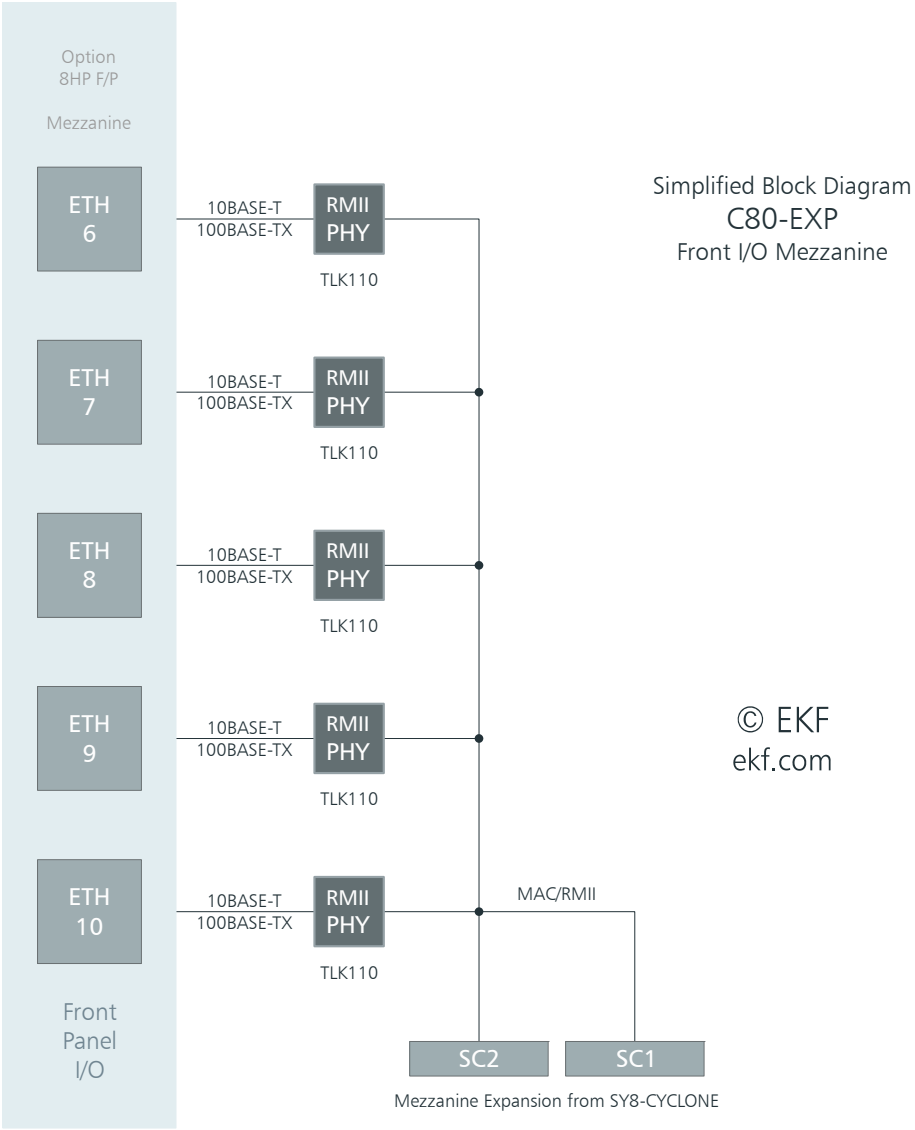
Feature Summary

Regulatory

- Long term availability
- Designed & manufactured in Germany
- ISO 9001 certified quality management
- Rugged solution (coating, sealing, underfilling on request)
- RoHS compliant
- Industrial operation temperature range -40°C to +85°C
- Humidity 5% ... 95% RH non condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF 24.8 years
- EC Regulations EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1)

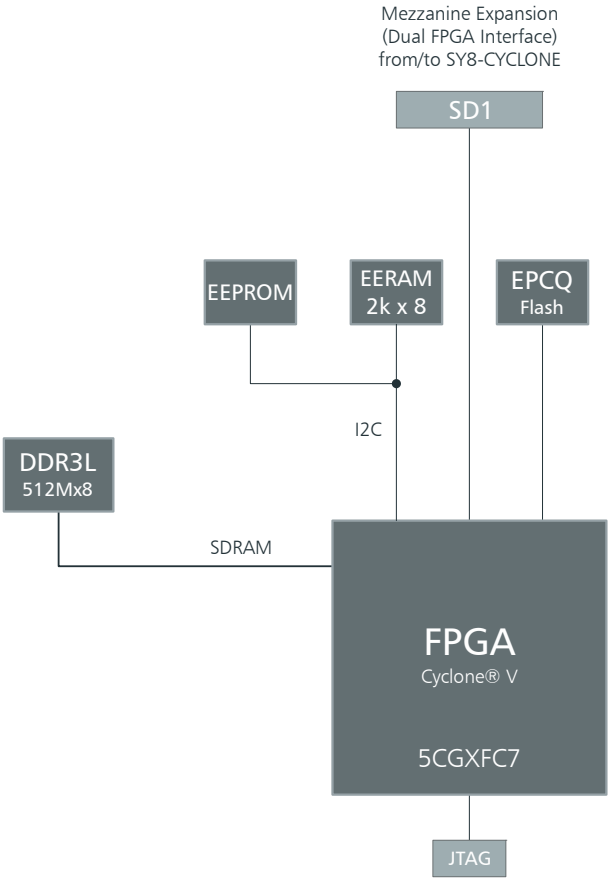
Block Diagram



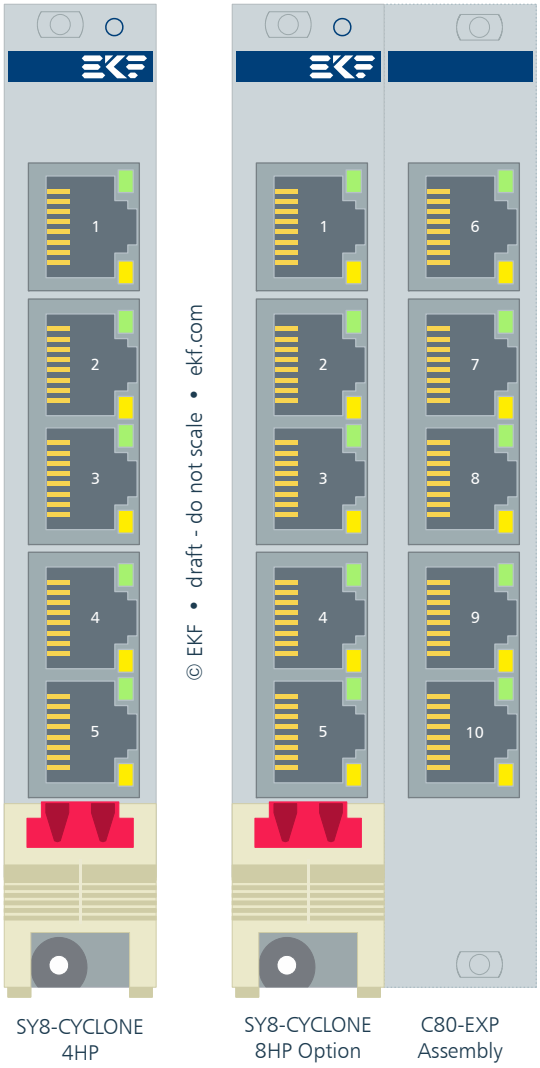


Simplified Block Diagram
C80-EXP
Front I/O Mezzanine

Simplified Block Diagram
C81-SI
FPGA Mezzanine

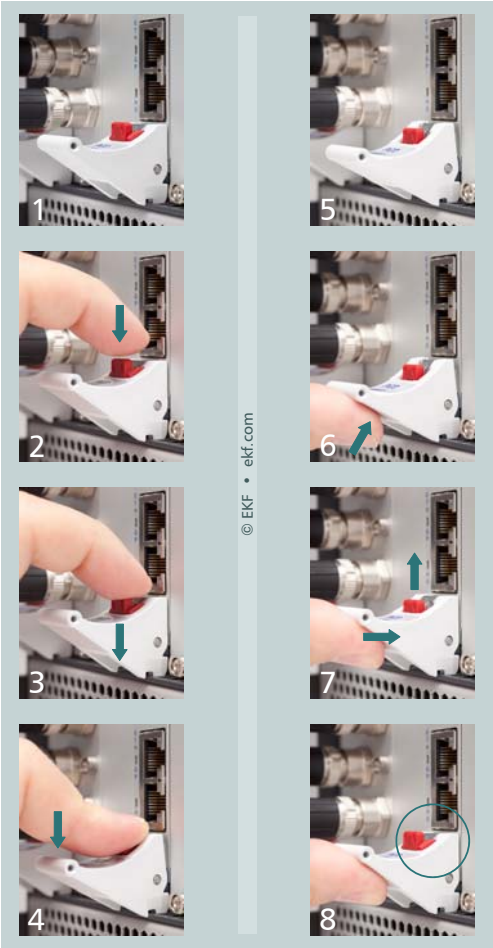


Front Panel



LEDs (per port): green=ACT, yellow=LNK

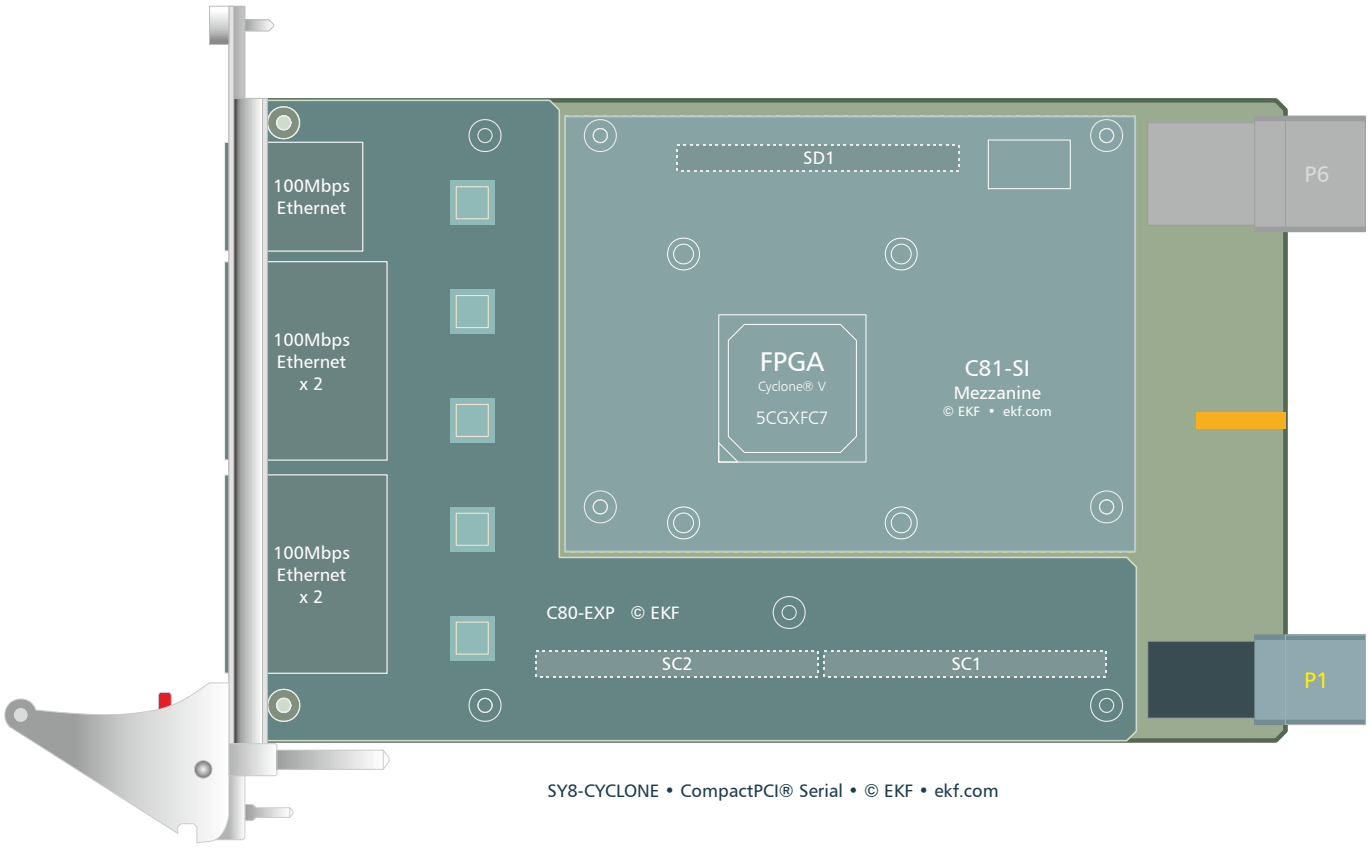
Please note: The front handle is provided with a built-in microswitch, which is used to disable the on-board power circuit when released. Vice versa, the *on-board devices are enabled not before the handle gets locked*. Please refer to the illustration below and make sure that the eject lever has reached its final position for proper board operation, as shown in picture 8. A gentle click should be audible, when the red actuator pin moves into its raised position, indicating that the board is locked and ready for use.



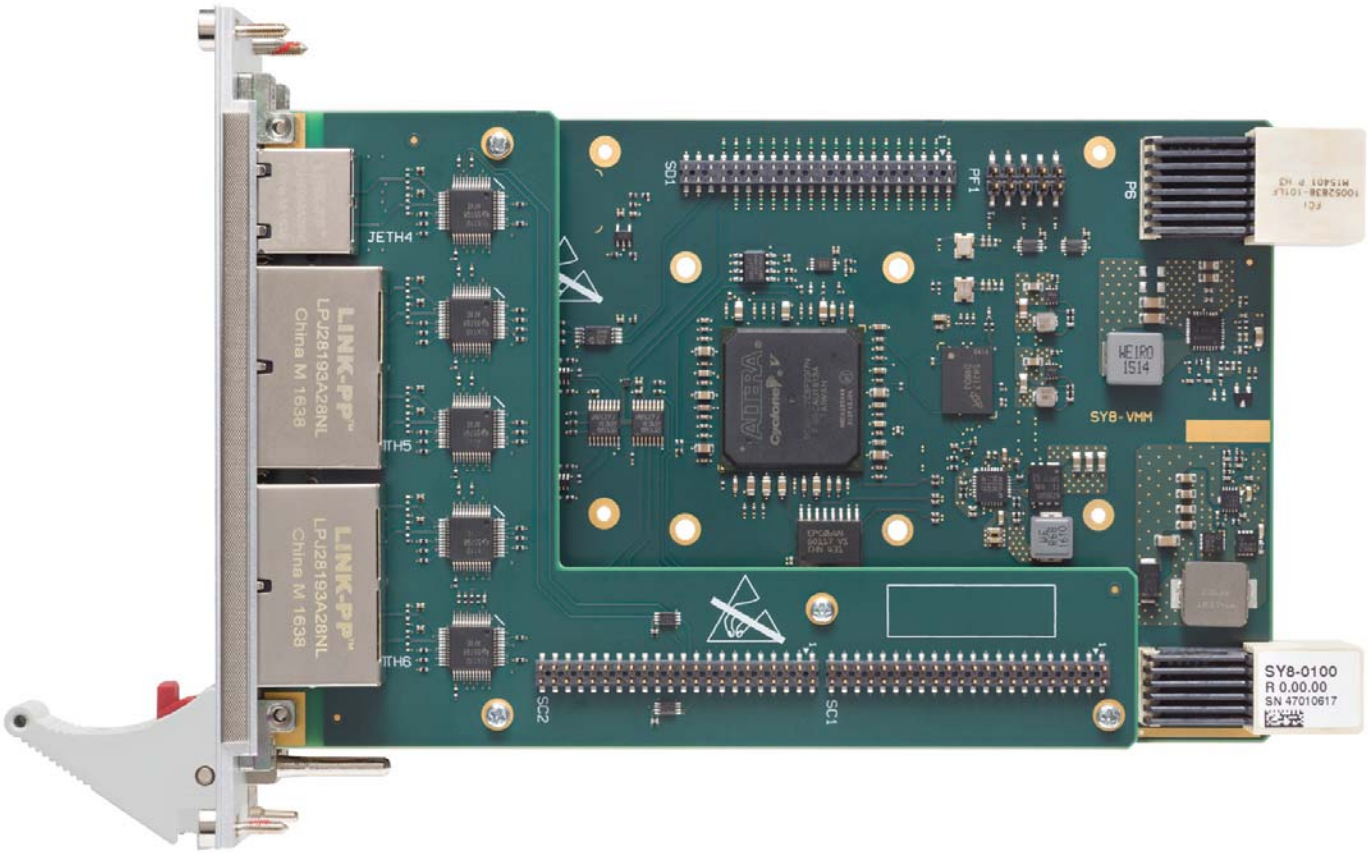
1 - 4: remove board
5 - 8: install board

1 & 8: on-board power enabled
2-7: on-board power disabled

Component Assembly



SY8-CYCLONE • CompactPCI® Serial • © EKF • ekf.com



FPGA

The SY8-CYCLONE is a universal hardware platform for FPGA based industrial networking and was designed for proprietary applications, to be specified by the customer.

The SY8-CYCLONE is equipped with a CYCLONE® V FPGA (Altera/Intel®). The board is normally populated with a 5CGXFC7C6F23I7N. There are several programmable interface blocks wired from the FPGA to on-board connectors and components:

- PCI Express® (hard IP), four lanes tied to the CompactPCI® Serial backplane connector P1 for host communication with the CPU card
- Five on-board 100Mbps Industrial Ethernet PHYs
- Five optional 100Mbps Industrial Ethernet PHYs by means of the C80-EXP mezzanine module (via SC1/SC2 connectors, alternate usage as custom specific signals)
- Interface connector SD1 for a secondary FPGA mezzanine module C81-SI, or alternate usage as auxiliary signals connector, for debug and/or custom specific I/O
- Memory interfaces to DDR3L RAM and I2C NV storage devices (EEPROM & FRAM)

A complete SY8-CYCLONE FPGA reference design for the Intel® Quartus® Prime suite is available, as a starting point for custom specific application programming, and in addition a Linux based test tool.

FPGA Default Signal Usage

Name	Bk	Pin	Type
PE_CLKIN+		V4	I
PE_CLKIN-		U4	I
1_PE_TX00+		Y4	O
1_PE_TX00-		Y3	O
1_PE_RX00+		AA2	I
1_PE_RX00-		AA1	I
1_PE_TX01+		U2	O
1_PE_TX00-		U1	O
1_PE_RX01+		W2	I
1_PE_RX01-		W1	I
1_PE_TX02+		N2	O
1_PE_TX02-		N1	O
1_PE_RX02+		R2	I
1_PE_RX02-		R1	I
1_PE_TX03+		J2	O
1_PE_TX03-		J1	O
1_PE_RX03+		L2	I
1_PE_RX03-		L1	I
PHY1_TX_EN	7	K20	O
PHY1_TXD1	5	K22	O
PHY1_TXD0	5	K21	O
PHY1_RX_CLK	7	G21	I
PHY1_RX_DV	7	G22	I
PHY1_RXD1	7	J22	I
PHY1_RXD0	7	J21	I
PHY1_CRS/RX_DV	7	H20	I
PHY1_CLK	7	H16	O
PHY1_ RST#	7	G20	O
PHY1_LINK	7	F22	I
PHY2_TX_EN	7	E21	O
PHY2_TXD1	7	F20	O
PHY2_TXD0	7	E22	O
PHY2_RX_CLK	7	B22	I
PHY2_RX_DV	7	C20	I
PHY2_RXD1	7	E20	I
PHY2_RXD0	7	D22	I
PHY2_CRS/RX_DV	7	C21	I
PHY2_CLK	7	H13	O
PHY9_CLK	8	F10	O
PHY9_ RST#	7	G12	O
PHY9_LINK	7	F12	I
PHY10_TX_EN	7	E12	O

Name	Bk	Pin	Type
PHY2_RST#	7	B21	O
PHY2_LINK	7	B20	I
PHY3_TX_EN	7	A19	O
PHY3_TXD1	7	A22	O
PHY3_TXD0	7	A20	O
PHY3_RX_CLK	7	C18	I
PHY3_RX_DV	7	C19	I
PHY3_RXD1	7	A18	I
PHY3_RXD0	7	A17	I
PHY3_CRS/RX_DV	7	B17	I
PHY3_CLK	8	G10	O
PHY3_RST#	7	D19	O
PHY3_LINK	7	D17	I
PHY4_TX_EN	7	F18	O
PHY4_TXD1	7	E19	O
PHY4_TXD0	7	F19	O
PHY4_RX_CLK	7	J17	I
PHY4_RX_DV	7	J18	I
PHY4_RXD1	7	G18	I
PHY4_RXD0	7	G17	I
PHY4_CRS/RX_DV	7	J19	I
PHY4_CLK	7	H15	O
PHY4_RST#	7	A15	O
PHY4_LINK	7	B16	I
PHY5_TX_EN	7	C15	O
PHY5_TXD1	7	B15	O
PHY5_TXD0	7	C16	O
PHY5_RX_CLK	7	G16	I
PHY5_RX_DV	7	F14	I
PHY5_RXD1	7	E16	I
PHY5_RXD0	7	E15	I
PHY5_CRS/RX_DV	7	F15	I
PHY5_CLK	5	M16	O
PHY5_ RST#	7	G15	O
PHY5_LINK	7	H14	I
PHY6_TX_EN	3A	U7	O
PHY6_TXD1	3A	P7	O
PHY6_TXD0	3A	W8	O
DEBUG27	5	L19	I/O
DEBUG28	7	K19	I/O
DEBUG29	7	H11	I/O
DEBUG30	7	H21	I/O

Name	Bk	Pin	Type
PHY6_RX_CLK	3A	W9	I
PHY6_RX_DV	3A	V6	I
PHY6_RXD1	3A	U6	I
PHY6_RXD0	3A	T7	I
PHY6_CRS/RX_DV	3A	R5	I
PHY6_CLK	3A	R6	O
PHY6_ RST#	3A	R7	O
PHY6_LINK	3A	P6	I
PHY7_TX_EN	3A	N6	O
PHY7_TXD1	3A	M6	O
PHY7_TXD0	3A	M7	O
PHY7_RX_CLK	8	L7	I
PHY7_RX_DV	8	K7	I
PHY7_RXD1	8	H6	I
PHY7_RXD0	8	G6	I
PHY7_CRS/RX_DV	8	F7	I
PHY7_CLK	8	E10	O
PHY7_ RST#	8	E7	O
PHY7_LINK	8	E9	I
PHY8_TX_EN	8	B5	O
PHY8_TXD1	8	A5	O
PHY8_TXD0	8	D6	O
PHY8_RX_CLK	8	C6	I
PHY8_RX_DV	8	B6	I
PHY8_RXD1	8	B7	I
PHY8_RXD0	8	A7	I
PHY8_CRS/RX_DV	8	C8	I
PHY8_CLK	8	F9	O
PHY8_ RST#	8	A8	O
PHY8_LINK	8	D9	I
PHY9_TX_EN	8	C9	O
PHY9_TXD1	8	A9	O
PHY9_TXD0	8	B10	O
PHY9_RX_CLK	8	A10	I
PHY9_RX_DV	7	J11	I
PHY9_RXD1	7	G11	I
PHY9_RXD0	7	C11	I
PHY9_CRS/RX_DV	7	B11	I
MEM_DQ4	4	Y14	I/O
MEM_DQ5	4	Y15	I/O
MEM_DQ6	4	AA15	I/O
MEM_DQ7	4	AB17	I/O

FPGA Default Signal Usage

Name	Bk	Pin	Type
PHY10_TXD1	7	D12	O
PHY10_TXD0	7	B12	O
PHY10_RX_CLK	7	A12	I
PHY10_RX_DV	7	J13	I
PHY10_RXD1	7	D13	I
PHY10_RXD0	7	C13	I
PHY10_CRS/RX_DV	7	B13	I
PHY10_CLK	7	G13	O
PHY10_ RST#	7	A13	O
PHY10_LINK	7	A14	I
MDIO	5	L22	I/O
MDC	5	M22	O
DEBUG0	7	H18	I/O
DEBUG1	7	L8	I/O
DEBUG2	7	K9	I/O
DEBUG3	8	J8	I/O
DEBUG4	8	J9	I/O
DEBUG5	8	H8	I/O
DEBUG6	8	H9	I/O
DEBUG7	8	G8	I/O
DEBUG8	7	H10	I/O
DEBUG9	5	T15	I/O
DEBUG10	5	R15	I/O
DEBUG11	5	P16	I/O
DEBUG12	7	K16	I/O
DEBUG13	3A	U8	I/O
DEBUG14	5	P17	I/O
DEBUG15	5	P18	I/O
DEBUG16	5	M18	I/O
DEBUG17	5	L18	I/O
DEBUG18	5	T19	I/O
DEBUG19	5	T20	I/O
DEBUG20	5	T22	I/O
DEBUG21	5	R21	I/O
DEBUG22	5	P19	I/O
DEBUG23	5	R16	I/O
DEBUG24	5	N19	I/O
DEBUG25	5	M20	I/O
DEBUG26	5	M21	I/O

Name	Bk	Pin	Type
DEBUG31	7	B18	I/O
FPGA_SAFETY	5	T17	I/O
BROWN_OUT	8	J7	I/O
I2C_SDA	7	F13	I/O
I2C_SCL	7	E14	I/O
CLK50	5	N16	I
CLK100	3A	T8	I
MEM_RST#	4	W21	O
MEM_CK	3B	U12	O
MEM_CK#	3B	U11	O
MEM_ODT	4	AA13	O
MEM_CS#	3B	N8	O
MEM_CKE	4	AA19	O
MEM_A0	3B	AA12	O
MEM_A1	3B	Y11	O
MEM_A2	3B	AB11	O
MEM_A3	3B	AB10	O
MEM_A4	3B	R11	O
MEM_A5	3B	R10	O
MEM_A6	3B	P12	O
MEM_A7	3B	R12	O
MEM_A8	3B	U10	O
MEM_A9	3B	T9	O
MEM_A10	3B	AB8	O
MEM_A11	3B	AA8	O
MEM_A12	3B	AB7	O
MEM_A13	3B	AA7	O
MEM_A14	3B	V10	O
MEM_A15	3B	V9	O
MEM_BA0	3B	Y9	O
MEM_BA1	3B	R9	O
MEM_BA2	3B	T10	O
MEM_RAS#	3B	AA10	O
MEM_CAS#	3B	AA9	O
MEM_WE#	3B	AB5	O
MEM_DQ0	4	V13	I/O
MEM_DQ1	4	U13	I/O
MEM_DQ2	4	AB12	I/O
MEM_DQ3	4	AA14	I/O

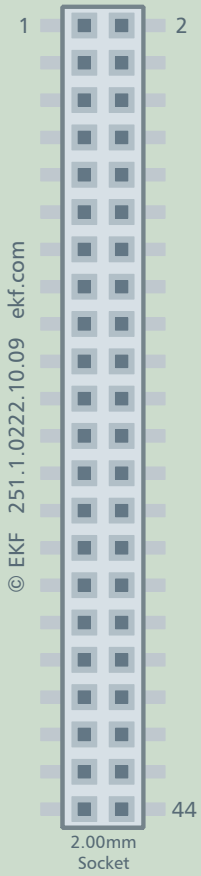
Name	Bk	Pin	Type
MEM_DQS	4	T13	I/O
MEM_DQS#	4	T12	I/O
EEP_SCL	5	N20	O
EEP_SDA	5	N21	I/O
FRAM_SCL	5	K17	O
FRAM_SDA	5	L17	I/O

Mezzanine Connectors SC1/SC2

As an option, the SY8-CYCLONE can be expanded by the C80-EXP front panel I/O mezzanine module, which is provided with five more Ethernet PHYs and RJ45 receptacles. The expansion module fits on the connectors SC1/SC2, for a mechanical pitch of 4HP (8HP front panel assembly in total for the SY8-CYCLONE base card and the C80-EXP mezzanine module).

As an alternate, the connectors SC1/SC2 may be used for custom specific I/O.

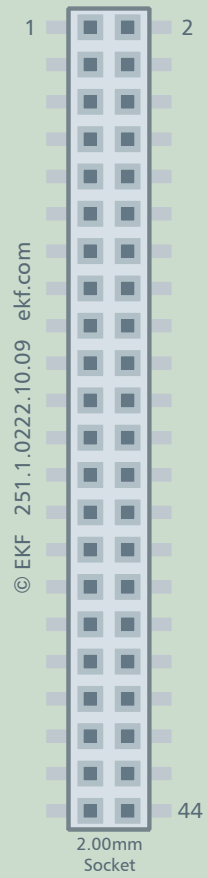
SC1 • Front I/O Mezzanine Expansion Interface
2.00mm Socket 2 x 22 (251.1.0222.10.09)



+3.3V	1	2	GND
+3.3V	3	4	GND
+3.3V	5	6	GND
PHY6_TX_EN	7	8	PHY6_TXD1
PHY6_TXD0	9	10	PHY6_RX_CLK
PHY6_RX_DV	11	12	PHY6_RXD1
PHY6_RXD0	13	14	PHY6_CRS/RX_DV
PHY6_CLK	15	16	PHY6_ RST#
PHY6_LINK	17	18	PHY7_TX_EN
PHY7_TXD1	19	20	PHY7_TXD0
PHY7_RX_CLK	21	22	PHY7_RX_DV
PPHY7_RXD1	23	24	PHY7_RXD0
PHY7_CRS/RX_DV	25	26	PHY7_CLK
PHY7_ RST#	27	28	PHY7_LINK
PHY8_TX_EN	29	30	PHY8_TXD1
PHY8_TXD0	31	32	PHY8_RX_CLK
PHY8_RX_DV	33	34	PHY8_RXD1
PHY8_RXD0	35	36	PHY8_CRS/RX_DV
PHY8_CLK	37	38	PHY8_ RST#
PHY8_LINK	39	40	PHY9_TX_EN
PHY9_TXD1	41	42	PHY9_TXD0
PHY9_RX_CLK	43	44	PHY9_RX_DV

SC2 • Front I/O Mezzanine Expansion Interface

2.00mm Socket 2 x 22 (251.1.0222.10.09)



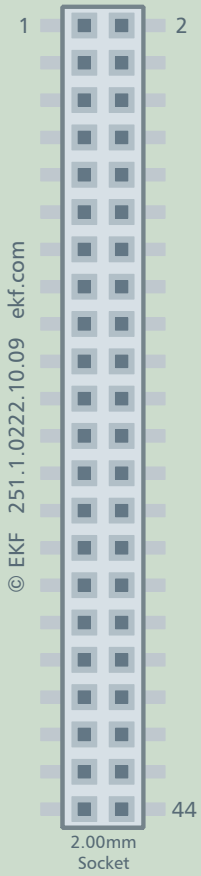
PHY9_RXD1	1	2	PHY9_RXD0
PHY9_CRS/RX_DV	3	4	PHY9_CLK
PHY9_ RST#	5	6	PHY9_LINK
PHY10_TX_EN	7	8	PHY10_TXD1
PHY10_TXD0	9	10	PHY10_RX_CLK
PHY10_RX_DV	11	12	PHY10_RXD1
PHY10_RXD0	13	14	PHY10_CRS/RX_DV
PHY10_CLK	15	16	PHY10_ RST#
PHY10_LINK	17	18	MDIO
MDC	19	20	TDO_PHY5 (TDI_PHY6)
TMS	21	22	TDO_PHY10
GND	23	24	GND
TCK_PHY6	25	26	GND
GND	27	28	GND
TCK_PHY7	29	30	GND
GND	31	32	GND
TCK_PHY8	33	34	GND
GND	35	36	GND
TCK_PHY9	37	38	GND
GND	39	40	GND
TCK_PHY10	41	42	GND
GND	43	44	GND

Mezzanine Connector SD1

As an option, the SY8-CYCLONE can be expanded by the C81-SI FPGA mezzanine module, for a secondary FPGA. The FPGA module fits on the connector SD1, with a suggested mechanical pitch of 4HP (8HP front panel assembly in total for the SY8-CYCLONE base card and the C81-SI mezzanine module).

As an alternate, the connector SD1may be used for test and debug, or custom specific I/O.

SD1 • Front I/O Mezzanine Expansion Interface
2.00mm Socket 2 x 22 (251.1.0222.10.09)



DEBUG0	1	2	DEBUG1
DEBUG2	3	4	DEBUG3
DEBUG4	5	6	DEBUG5
DEBUG6	7	8	DEBUG7
DEBUG8	9	10	DEBUG9
DEBUG10	11	12	DEBUG11
DEBUG12	13	14	DEBUG13
DEBUG14	15	16	DEBUG15
DEBUG16	17	18	DEBUG17
DEBUG18	19	20	DEBUG19
DEBUG20	21	22	DEBUG21
DEBUG22	23	24	DEBUG23
DEBUG24	25	26	DEBUG25
DEBUG26	27	28	DEBUG27
DEBUG28	29	30	DEBUG29
DEBUG30	31	32	DEBUG31
DEBUG_SAFETY	33	34	BROWN_OUT
I2C_SDA	35	36	FPGA_SAFETY
I2C_SCL	37	38	GND
+3.3V	39	40	GND
+3.3V	41	42	GND
+3.3V	43	44	GND

P1 CompactPCI® Serial Backplane Connector

P1 CompactPCI® Serial Peripheral Slot Backplane Connector EKF Part #250.3.1206.20.02 • 72 pos. 12x6, 14mm Width												
P1	A	B	C	D	E	F	G	H	I	J	K	L
6	GND	1 PE TX02+	1 PE TX02-	GND	1 PE RX02+	1 PE RX02-	GND	1 PE TX03+	1 PE TX03-	GND	1 PE RX03+	1 PE RX03-
5	1 PE TX00+	1 PE TX00-	GND	1 PE RX00+	1 PE RX00-	GND	1 PE TX01+	1 PE TX01-	GND	1 PE RX01+	1 PE RX01-	GND
4	GND	*1_ USB2+*	*1_ USB2-*	GND	PE_CLK IN+	PE_CLK IN-	GND	*1 SATA TX+*	*1 SATA TX-*	GND	*1 SATA RX+*	*1 SATA RX-*
3	*1 USB3 TX+*	*1 USB3 TX-*	GA0	*1 USB3 RX+*	*1 USB3 RX-*	GA1	*SATA SDI*	*SATA SDO*	GA2	*SATA SCL*	*SATA SL*	GA3
2	GND	I2C SCL	I2C SDA	GND	*RSV*	*RSV*	GND	RST#	WAKE#	GND	PE_ EN#	SYS EN#
1	+12V	STBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

pin positions printed white/italic: not connected

For signal descriptions please refer to PICMG CPCI-S.0 R1.0 CompactPCI® Serial Specification

Related Documents

Reference Documents		
Term	Document	Origin
CompactPCI® Serial	CPCI-S.0	www.picmg.org
CYCLONE® V	Intel® Cyclone V Device Datasheet CV-51002 and other design resources	www.altera.com

Ordering Information

Ordering Information
For popular SY8-CYCLONE SKUs please refer to www.ekf.com/liste/liste_21.html#SY8

Beyond All Limits:
EKF High Performance Embedded

Industrial Computers Made in Germany

boards. systems. solutions.

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